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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,759	04/14/2004	Kuo-Rong Chen	OP-093000122	5064
7590		02/06/2006	EXAMINER	
Yi-Wen Tseng		SANEI, HANA ASMAT		
4331 Stevens Battle Lane		ART UNIT		
Fairfax, VA 22033		PAPER NUMBER		
		2879		

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/823,759

Applicant(s)

CHEN ET AL.

Examiner

Hana A. Sanei

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 January 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) 11-17 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☒ Claim(s) 1,6-7 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Election/Restrictions***

Applicant's election, filed on 1/12/06, was made without traverse to prosecute the invention drawn to FED device, claims 1-10. Claims 11-17 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

### ***Claim Objections***

Claims 1, 6- 7 are objected to because of the following informalities:

Claim 1 lacks antecedent basis regarding the phrase "first conductive plate;" Examiner believes applicant is referring to the "first conductive layer," but is unsure. For purposes of examination, Examiner will view both the "first conductive plate" and the "first conductive layer" as one single element.

Regarding Claim 6, the term "glass glue" is not elaborate and may be interpreted broadly; the term is not elaborated on in the applicant's disclosure.

Claim 7 lacks antecedent basis regarding the "insulation layer" of Page 10, line 5. For purposes of examination, the "insulation layer" as claimed will be identified as the same "insulation layer" of Page 10, lines 7 & 10.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakai et al (US 6057636).

With respect to Claim 1, Sakai teaches a first conductive layer (inducing electrode, 40, see at least Fig. 10) to serve as a converging electrode layer having a proximal surface facing the anode units (16) and a distal surface opposing to the proximal surface, the first conductive plate comprising a plurality of first apertures (refer to Fig. 10) extending therethrough; a glass plate (15, SiO<sub>2</sub>; Col. 10, lines 45-46) formed, the glass plate including a plurality of second apertures extending therethrough (refer to abovementioned Figure); an insulation layer (insulating spacer layer, 41) formed on the distal surface of the first conductive layer; and a second conductive layer (14) formed on the insulation layer to serve as a gate electrode layer, the second conductive layer having a proximal surface facing the cathode units (11) and a distal surface opposing to the proximal surface, wherein the second conductive layer includes a plurality of third apertures extending therethrough and aligned with the first and second apertures (refer to abovementioned Figure).

With respect to Claim 2, Sakai teaches that each second aperture is aligned with one corresponding first aperture (see Fig. 10).

With respect to Claim 3, Sakai teaches that each second aperture covers an opening range of a plurality of the first apertures (see Fig. 10).

With respect to Claim 4, Sakai teaches that each third aperture is aligned with one corresponding first aperture (see Fig. 10).

With respect to Claim 5, Sakai teaches that each third aperture covers an opening range of a plurality of the first apertures (see Fig. 10).

With respect to Claim 6, Sakai teaches that the insulation layer is a glass glue (41; silicon oxide film, Col. 11, lines 13-15).

With respect to Claim 7, Sakai teaches a converging electrode layer (inducing electrode, 40, see at least Fig. 10) having an array of first apertures extending therethrough; a spacing glass plate (15, SiO<sub>2</sub>; Col. 10, lines 45-46) located adjacent to one side of the converging electrode layer, the insulation layer (insulating spacer layer, 41) having a plurality of second apertures aligned with the first apertures and formed on the other side of the converging electrode layer; and a gate layer (14) including a plurality of conductive lines (portions encompassing apertures) located adjacent to the insulation layer, wherein each of the conductive lines is aligned with a portion of the converging electrode layer between one pair of neighboring rows of the first apertures (see Fig. 12). That Sakai's gate layer is provided with predetermined separate apertures implies the inherency of providing the gate layer with conductive "lines."

With respect to Claim 8, Sakai teaches that the gate layer (14) further comprises a hollow frame (aperture) within which the conductive lines extend (non-apertured portions Fig. 10). It should be noted that Sakai's hollow frame is apertures-conductive line-aperture combination implies that the conductive lines extend within.

With respect to Claim 9, Sakai teaches that the second apertures are aligned with one corresponding first aperture (Fig. 10).

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With respect to Claim 10, Sakai teaches that each of the second apertures is aligned with a plurality of corresponding first apertures (Fig. 10).

***Other Sited Prior Art***

Ono et al (US 6456014 B1) teaches the pixilated formation of emitters of a field emission display.

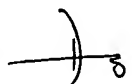
***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hana A. Sanei whose telephone number is (571) 272-8654. The examiner can normally be reached on Monday- Friday, 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner

 2/2/06

Hana A. Sanei

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